IN THE CLAIMS

Applicant submits below a complete listing of the current claims, including marked-up claims with insertions indicated by underlining and deletions indicated by strikeouts and/or double bracketing. This listing of claims will replace all prior versions, and listings, of claims in the application:

Claims

1. (Original) A method for testing in parallel several identical integrated circuit chips with an asynchronous operation, via two physical contacts between a tester and each of the chips, comprising:

transmitting on the tester side a first test control signal for the integrated circuit chips;

having the test executed in desynchronized fashion by each of the integrated circuit chips;

transmitting on the tester side, after a predetermined time interval following the transmission of the first control signal, a second result request control signal to the integrated circuit chips; and

having all chips respond synchronously upon reception of said second control signal.

2. (Original) The method of claim 1, wherein the predetermined time interval is selected to be longer than the maximum execution time of the test steps by any integrated circuit chip.

3. (Original) The method of claim 1, wherein an integrated circuit chip receiving said first control signal sets, after desynchronized execution of the test steps, to a state ready to accept a synchronized answer control signal.

4. (Original) The method of claim 1, wherein the test is considered as being negative as soon as the expected binary answer differs from a predetermined data word stored on the tester side.

5. (Original) A system for testing by twin-wire contact a set of identical integrated circuit chips in parallel fashion, comprising:

a device capable of implementing the method of claim 1.

6. (Original) The system of claim 5, wherein each integrated circuit chip to be tested is capable of interpreting at least one control signal to switch to a synchronous operating mode.

7. (New) A method for testing in parallel several integrated circuit chips designed for asynchronous operation, using two physical contacts between a tester and each of the chips, comprising:

transmitting, from the tester a first test control signal to the integrated circuit chips;

having the test executed by each of the integrated circuit chips without synchronizing operation of the integrated circuit chips;

transmitting, from the tester, after a time interval following the transmission of the first test control signal, a second result request control signal to the integrated circuit chips; and

having all chips respond synchronously upon reception of said second control signal.

8. (New) The method of claim 7, wherein the time interval is selected to be longer than the maximum execution time of the test steps by any integrated circuit chip.

9. (New) The method of claim 7, wherein an integrated circuit chip receiving said first control signal sets, after execution of the test steps, to a state ready to accept a synchronized answer control signal.

10. (New) The method of claim 7, wherein the test is considered as being negative as soon as the expected binary answer differs from a data word stored on the tester side.

11. (New) A system for testing a set of identical integrated circuit chips in parallel, comprising:

a plurality of physical contact pairs intended to contact pads of the respective chips; and

a device capable of:

transmitting, from the tester a first test control signal to the integrated circuit chips;

having the test executed by each of the integrated circuit chips without synchronizing operation of the integrated circuit chips;

transmitting, from the tester, after a time interval following the transmission of the first test control signal, a second result request control signal to the integrated circuit chips; and

having all chips respond synchronously upon reception of said second control signal.

12. (New) The system of claim 11, wherein each integrated circuit chip to be tested is capable of interpreting at least one control signal to switch to a synchronous operating mode.